ECE 451-LAB5

Fall 2019

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# List of items completed

* 1. Design of positive edge triggered D-Flip Flop
  2. Design of Grey Code Counter

# Lab Procedures

* 1. Grey code Counter state transition diagram

100

000

001

101

011

111

110

010

* 1. State transition table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Present State | | |  | Next State | | |
| **Q2** | **Q1** | **Q0** |  | **Q2** | **Q1** | **Q0** |
| 0 | 0 | 0 |  | 0 | 0 | 1 |
| 0 | 0 | 1 |  | 0 | 1 | 1 |
| 0 | 1 | 1 |  | 0 | 1 | 0 |
| 0 | 1 | 0 |  | 1 | 1 | 0 |
| 1 | 1 | 0 |  | 1 | 1 | 1 |
| 1 | 1 | 1 |  | 1 | 0 | 1 |
| 1 | 0 | 1 |  | 1 | 0 | 0 |
| 1 | 0 | 0 |  | 0 | 0 | 0 |

* 1. K-maps for D in put of the flip flop

D2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q2\Q1,Q0 | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 |

D1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q2\Q1,Q0 | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |

D0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q2\Q1,Q0 | 00 | 01 | 11 | 10 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |

The lab design starts with designing of a D- Flip Flop. Then followed by creating a combinational logic based on the equation generated in above table

# Schematics/Verilog models

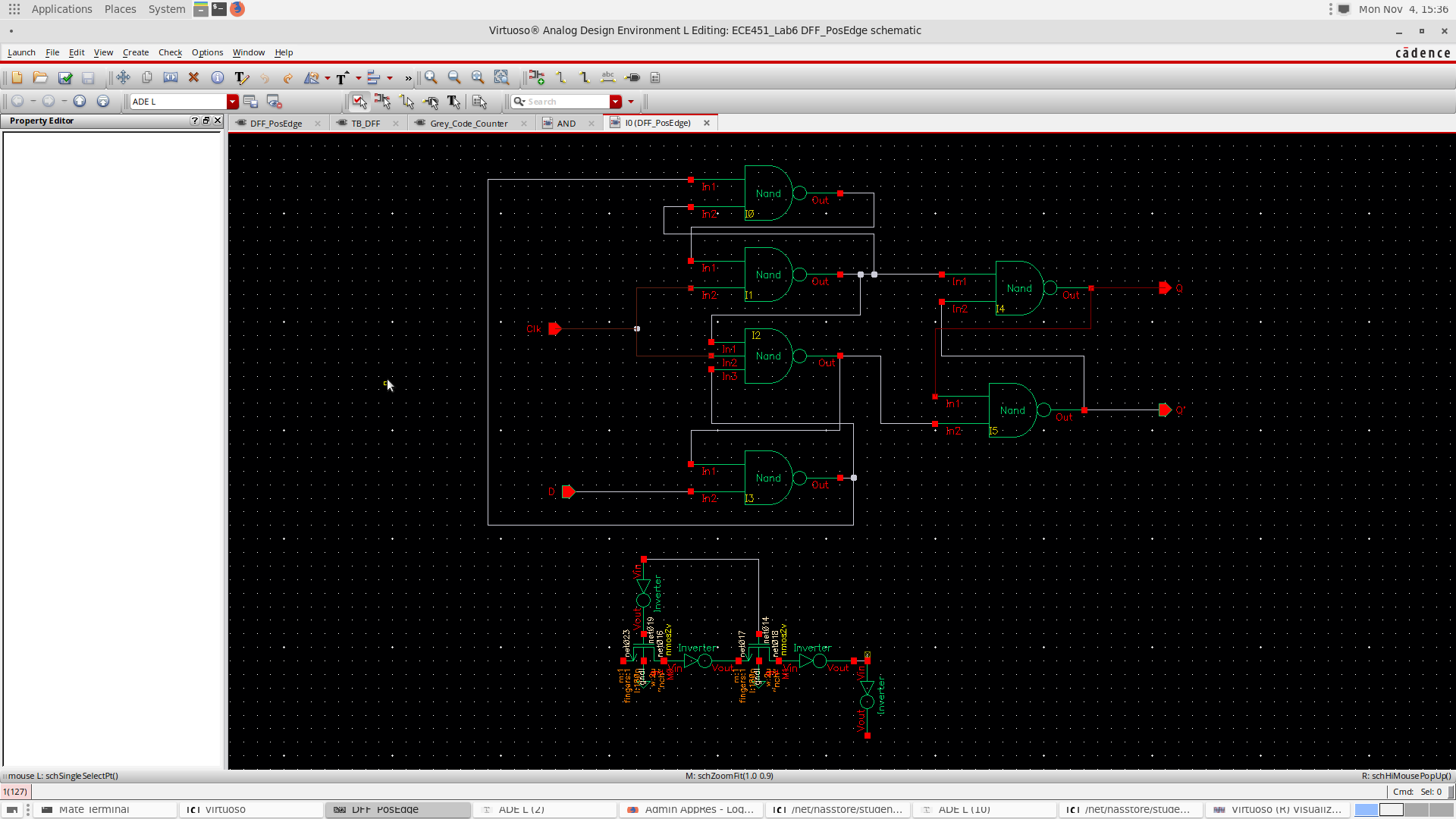


Figure : D-Flip Flop Schematic using gates

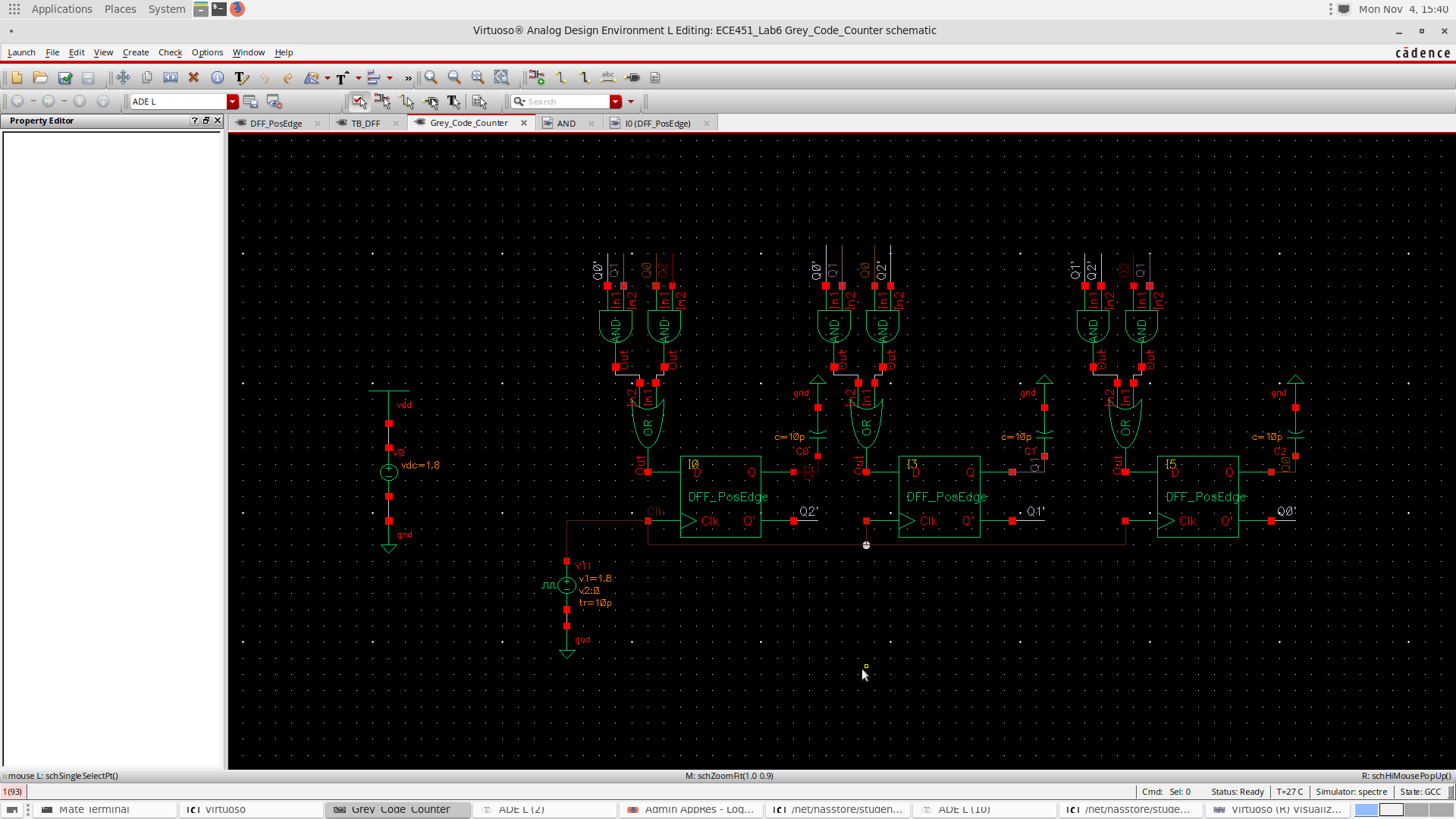


Figure : Grey Code Counter using D-Flip Flop

# Simulation Results



Figure : Simulation Results

# Analysis and Explanations

The simulation results clearly follow the grey code counter sequence. As we didn’t design a condition for initial state, the counter randomly enters a state and starts up counting from that state following the Grey code counter sequence.

# Conclusion

In this LAB we have successfully designed a 3-bit grey code counter using D-Flip Flops and understand the concept of sequential circuit design.

# Answers to questions posted in the lab

**Q) What is Moore Finite State Machine(FSM)?**

Moore finite state machine is a system whose outputs are decided only based on its current state. The outputs are decided based on the state.

**Q) What is Mealy FSM?**

Mealy FSM is a system whose outputs are decided based on the inputs and the current state. The outputs are set on the transition between states.